Listing of the Claims

1. (Currently Amended): A computer-implemented method for designing circuits, comprising:

receiving a register transfer level (RTL) textual description of a circuit design model as input to a logical synthesis stage; and

performing logical synthesis using the RTL textual description, the logical synthesis being performed before assigning physical locations to the circuits, wherein performing logical synthesis comprises:

generating a logic network from the RTL textual description of the circuit design model;

determining a structural metric through an analysis of the logic network, wherein the structural metric is a measure of wiring congestion of the circuit design model ~~after physical design~~; and

using the structural metric during the logical synthesis ~~stage~~ to predict wiring congestion of the circuit design model ~~after the physical design~~ to optimize the circuit design model.

2. (Previously Presented): The method of claim 1, wherein using the structural metric to optimize the circuit design model comprises adding, deleting or substituting one or more circuits using a combination of boolean, algebraic and electrical optimizations.

3. (Previously Presented): The method of claim 1, wherein the structural metric includes a measure of routing congestion of the circuit design model after placement and routing, the routing congestion being measured by an average and a peak number of wires crossing any bisection of the placed and routed circuit design model.

4. (Previously Presented): The method of claim 1, wherein using the structural metric to optimize the circuit design model comprises using the structural metric during a technology independent synthesis stage of the logic synthesis stage.

5. (Previously Presented): The method of claim 1, wherein using the structural metric to optimize the circuit design model comprises using the structural metric during a technology mapping stage of the logic synthesis stage.

6. (Previously Presented): The method of claim 1, wherein using the structural metric to optimize the circuit design model comprises using the structural metric during a buffering stage of the logic synthesis stage.

7. (Previously Presented): The method of claim 1, further comprising incrementally updating the structural metric when logic changes are made to the circuit design model.

8. (Previously Presented): The method of claim 7, wherein incrementally updating the structural metric when logic changes are made to the circuit design model comprises performing recomputation on circuits involved in an optimization and circuits affected by the optimization to provide a structural metric cost.

9. (Previously Presented: The method as in claim 7, wherein incrementally updating the structural metric when logic changes are made to the circuit design model comprises maintaining information regarding circuits affected by an optimization, which are computed when recomputation of the structural metric is necessary.

10. (Previously Presented): The method of claim 1, wherein the structural metric comprises any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric.

11. (Previously Presented): The method of claim 1, wherein determining a structural metric comprises:

generating one or more possible optimizations;

incrementally updating the structural metric when the optimizations are made to the circuit design model to evaluate the cost of applying each of the one or more possible

optimizations to the circuit design model, the structural metric comprising any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric;

evaluating a structural metric cost of each of the one or more possible optimizations as given by the structural metric;

selecting an optimization from the one or more possible optimizations with the lowest structural metric cost; and

applying the optimization to the circuit design model.

12. (Original): The method of claim 11, wherein generating the one or more possible optimizations comprises:

generating a structure-driven kernel factoring;

generating a structure-driven decomposition;

generating a structure-driven tech mapping; and

generating a structure-aware buffering.

13. (Currently Amended): A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for optimizing a circuit design model the method steps comprising:

receiving a register transfer level (RTL) textual description of a circuit design model as input to a logical synthesis stage; and

performing logical synthesis using the RTL textual description, the logical synthesis being performed before assigning physical locations to the circuits, wherein performing logical synthesis comprises:

generating a logic network from the RTL textual description of the circuit design model;

determining a structural metric through an analysis of the logic network, wherein the structural metric is a measure of wiring congestion of the circuit design model ~~after physical design~~; and

using the structural metric during the logical synthesis ~~stage~~ to predict wiring congestion of the circuit design model ~~after the physical design~~ to optimize the circuit design model.

14. (Currently Amended): A system for designing circuits, comprising:

means for creating a structural metric from a logic network during ~~a~~ logical synthesis ~~stage~~ of a circuit design model, wherein the logic network is derived from a register transfer level (RTL) textual description of the circuit design model, and the structural metric is a measure of wiring congestion of the circuit design model ~~after physical design~~; and

means for using the structural metric during the logic synthesis ~~stage~~ to predict wiring congestion of the circuit design model ~~after the physical design~~ to optimize the circuit design model,

wherein the creating and using are performed before assigning physical locations to the circuits.

15. (Previously Presented): The program storage device of claim 13, wherein the structural metric includes a measure of routing congestion of the circuit design model after placement and routing, the routing congestion being measured by an average and a peak number of wires crossing any bisection of the placed and routed circuit design model.

16. (Previously Presented): The program storage device of claim 13, wherein the method steps further comprise incrementally updating the structural metric when logic changes are made to the circuit design model.

17. (Previously Presented): The program storage device of 16, wherein incrementally updating the structural metric when logic changes are made to the circuit design model comprises performing recomputation on circuits involved in an optimization and circuits affected by the optimization to provide a structural metric cost.

18. (Previously Presented): The program storage device of 16, wherein incrementally updating the structural metric when logic changes are made to the circuit design model comprises maintaining information regarding circuits affected by an optimization, which are computed when recomputation of the structural metric is

necessary.

19. (Previously Presented): The program storage device of 13, wherein the structural metric comprises any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric.

20. (Previously Presented): The program storage device of 13, wherein determining a structural metric comprises:

generating one or more possible optimizations;

incrementally updating the structural metric when the optimizations are made to the circuit design model to evaluate the cost of applying each of the one or more possible optimizations to the circuit design model, the structural metric comprising any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric;

evaluating a structural metric cost of each of the one or more possible optimizations as given by the structural metric;

selecting an optimization from the one or more possible optimizations with the lowest structural metric cost; and

applying the optimization to the circuit design model.